GoLogicPro™ Specifications

June 19, 2026

Specifications subject to change without notice.

Probes

Channel inputs

- 36 or 72 depending on model
- Timing mode: all channels are data inputs
- Differential input mode halves the data inputs
- State mode: 1 to 8 channels are clock inputs

Electrical characteristics

- Input impedance: 100 Kohm; 5 picofarads
- 1 nanosecond maximum skew between channels
- Each channel is coaxially shielded
- Ground-connect for each channel
- 8 separate ground-connect channels are also provided

Threshold levels

- 1 independent level per channel
- Range: 0V to 3.3V in 10 millivolt increments
- Accuracy: ≈ 50 millivolt around selected voltage level
- Minimum swing: 300 mv (±150 mv around active threshold)

Input voltage limits

- ± 12 volts
- Exceeding this limit may damage the GoLogicPro

Sample Rate Limits

The active sample mode and active pods define the maximum sample rate.

Sample Mode: Normal timing analysis

- Pods A, B, C, D: 1 GHz
- Pods A, B: 2.5 GHz
- Pod A: 4 GHz

Sample Mode: Transitional timing analysis

- Pods A, B, C, D: 900 MHz
- Pods A, B: 1.9 GHz

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- Pods A: 3.2 GHz

Sample Mode: Serial Bus Trigger

- Pod A: 500 MHz

Sample Mode: State analysis "1 to 8 clock inputs" mode

- Pods A, B, C, D: 100 MHz rising or falling edge (single data rate)
- Pods A, B, C, D: 50 MHz both edges (double data rate)
- Pods A, B: 100 MHz rising or falling edge (single data rate)
- Pods A, B: 50 MHz both edges (double data rate)
- Pods A: 200 MHz rising or falling edge (single data rate)
- Pods A: 100 MHz both edges (double data rate)

Sample Mode: State analysis "clock on A16/etc..." modes

- Source signal quality determines the maximum allowable frequency
- Maximum clock frequency: 300 MHz rising or falling edge (single data rate)
- Maximum clock frequency: 250 MHz both edges (double data rate)
- Channel C16 or D16 is clock input when 72 channels are active
- Channel A16 or B16 is clock input when 36 channels are active
- Clock on both edges available only when 36 channels are active
- The Phase Link Loop (PLL) cannot sync with clock signals below 1 MHz. Use the "1 to 8 clock input" option for clock signals 10 MHz and slower.
- The PLL cannot sync on non-periodic or asymmetric clock signals.
- A frequency counter detects the input clock signal's rate, and this value is used to display and scale the captured trace data.

Triggering

Events

- 32 value events
- 16 edge events

Timers / Counters

- Two 32-bit timers/counters per level

Levels

- 16 levels
- 3 If/Else lines per level
- 1 default "else" line per level
- 2 value events per level
- 1 edges events per level

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- 2 timers/counters per level

Actions

- Trigger (stop running)
- GoTo Level (1 to 16)

Selective Storage

- Available in Timing and State modes
- Available in Custom TriggerForm only
- Store all data while on a level, no data, or specified patterns

Resolution

- Sample rate ≥ 1 GHz: fixed at 2 ns
- Sample rate < 1 GHz: 1/2 sample rate
- State analysis "1 to 8 clock inputs": fixed at 8 ns on 72 channels
- State analysis "1 to 8 clock inputs": fixed at 4 ns on 36 channels
- State analysis "1 to 8 clock inputs": fixed at 4 ns on 18 channels
- State analysis "clock on A16/etc...": 1 input clock period

Trigger-out Signal

- Falling edge signal on trigger
- 3V when the logic analyzer starts running
- Changes from 3V to 0V when the logic analyzer triggers

Serial Bus Limits

- 1-Wire: header plus up to 5 bytes
- CAN / CAN-FD: header plus up to 7 bytes
- Clk+Data (bitstream): up to 14 bytes
- DMX512: up to 5 bytes
- eSPI: header plus up to 1 byte
- I2C: header plus up to 12 bytes
- I3C: header plus 1 byte
- I2S: up to 14 bytes
- JTAG: up to 7 bytes
- LIN: header plus up to 6 bytes
- LPC: up to 12 bytes
- MDIO / SMI: header plus up to 4 bytes
- ONFI SDR: header plus 1 byte
- PWM Encoder: 1 byte

- SDIO / MMC / eMMC: header plus up to 8 bytes
- SENT: up to 2 bytes
- SPI: up to 14 bytes
- Quad-SPI / SPI-MIO: header plus up to 8 data bytes
- UART: up to 6 bytes

Notes: Depending on bus type, data values can be contiguous or separated by nonmatching values. Some bus protocols infer that data values are always contiguous within a packet.

Also, fewer trigger values are available as the bit-width of each value increases. For example the SPI bus can be configured for 32-bit double words rather than 8-bit bytes. In that case, only 3 values can be in the trigger series.

Dimensions

Width: 4.5 in (115 mm)

Length: 4.75 in (118 mm)

Height: 1.5 in (35 mm)

Weight (main unit alone): 19 oz. (540 grams)

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