NCI *GoLogicXL*™ Specifications

October 1, 2021
Specifications subject to change without notice.

Probes

Channel inputs

- 36 or 72 depending on model
- Timing mode: all channels are data inputs
- Differential input mode halves the data inputs
- State mode: 1 to 8 channels are clock inputs

Electrical characteristics

- Input impedance: 50 Kohm; 4.5 picofarads
- 1 nanosecond maximum skew between channels
- Each channel is coaxially shielded
- Ground-connect for each channel
- 8 separate ground-connect channels are also provided

Threshold levels

- GoLogicXL-36: 2 independent levels
- GoLogicXL-72: 4 independent levels
- Range: 0V to 3.2V in 10 millivolt increments
- Accuracy: ≈ 50 millivolt around selected voltage level
- Minimum swing: 300 mv (±150 mv around active threshold)

Input voltage limits

- ± 12 volts
- Exceeding this limit may damage the GoLogicXL

Sampling

Normal timing analysis

- Maximum for 72 channels: 500 MHz
- Maximum for 36 channels: 1 GHz
- Maximum for 18 channels: 2 GHz
- Maximum for 9 channels: 4 GHz

Transitional timing analysis

- Maximum for 72 channels: 250 MHz
- Maximum for 36 channels: 500 MHz
- Maximum for 16 channels: 1 GHz
- Timestamp limits: see Appendix B for details

Glitch timing

- Maximum for 36 channels: 500 MHz

State analysis "1 to 8 clock inputs" mode

- Maximum for 72 channels: 50 MHz rising or falling edge (single data rate)
- Maximum for 72 channels: 25 MHz both edges (double data rate)
- Maximum for 36 channels: 100 MHz rising or falling edge (single data rate)
- Maximum for 36 channels: 50 MHz both edges (double data rate)
- Maximum for 16 channels: 200 MHz rising or falling edge (single data rate)
- Maximum for 16 channels: 100 MHz both edges (double data rate)

State analysis "clock on A16/etc..." modes

- Source signal quality determines the maximum allowable frequency.
- Maximum clock frequency: 300 MHz rising or falling edge (single data rate)
- Maximum clock frequency: 250 MHz both edges (double data rate)
- Channel C16 or D16 is clock input when 72 channels are active
- Channel A16 or B16 is clock input when 36 channels are active
- Clock on both edges available only when 36 channels are active
- The Phase Link Loop (PLL) cannot sync with clock signals slower than 1 MHz. Use the "1 to 8 clock input" option for clock signals 1 MHz and slower.
- The PLL cannot sync on non-periodic or asymmetric clock signals.
- A frequency counter detects the input clock signal's rate, and this value is used to display and scale the captured trace data.

SuperView™ trace overlay

- 16K samples
- Centered around trigger (8K samples before and 8K samples after main trigger)
- Available when 36 channels are active
- Available for Normal Timing, Transitional Timing, or State Analysis "1 to 8 clock inputs" modes are active
- Available using 100 MHz to 1 GHz main sampling rate
- Samples at 4X the main sample rate when Normal Timing is active (4 GHz max)
- Samples at 8X the main sample rate when Transitional Timing is active (4 GHz max)
- Disabled if fewer than 8K main trace samples are captured
- Disabled if no trigger event occurs
- Disabled if the trigger event is too close to the main trace start or end

Serial bus capture

- Maximum for 16 channels: 950 MHz

Sample depth (channels: maximum samples)

Normal timing analysis

Base memory option

- 72 channels: 34M samples
- 36 channels: 67M samples
- 18 channels: 134M samples
- 9 channels: 268M samples

Mid memory option

- 72 channels: 67M samples
- 36 channels: 134M samples
- 18 channels: 268M samples
- 9 channels: 536M samples

Large memory option ◦72 channels: 134M samples

- 36 channels: 268M samples
- 18 channels: 536M samples
- 9 channels: 1 billion samples

Transitional timing analysis

Base memory option

- 72 channels: 17M samples
- 36 channels: 34M samples
- 16 channels: 67M samples

Mid memory option

- 72 channels: 34M samples
- 36 channels: 67M samples
- 16 channels: 134M samples

Large memory option

- 72 channels: 67M samples
- 36 channels: 134M samples
- 16 channels: 268M samples

Glitch timing

Base memory option

- 36 channels: 34M samples

Mid memory option

- 36 channels: 67M samples

Large memory option

- 36 channels: 134M samples

State analysis "1 to 8 clock inputs"

Base memory option

- 72 channels: 17M samples
- 36 channels: 34M samples
- 16 channels: 67M samples

Mid memory option

- 72 channels: 34M samples
- 36 channels: 67M samples
- 16 channels: 134M samples

Large memory option

- 72 channels: 67M samples
- 36 channels: 134M samples
- 16 channels: 268M samples

State analysis "clock on A16/etc..."

Base memory option

- 72 channels: 34M samples
- 36 channels: 67M samples

Mid memory option

- 72 channels: 67M samples
- 36 channels: 134M samples

Large memory option

- 72 channels: 134M samples
- 36 channels: 268M samples

Serial bus capture

- Base memory option: 67M samples
- Mid memory option: 134M samples
- Large memory option: 268M samples

Triggering

Resolution

- Sample rate ≥ 1 GHz: fixed at 2 ns
- Sample rate < 1 GHz: 1/2 sample rate (4 ns at 500 MHz, 8 ns at 250 MHz,...)
- State analysis "1 to 8 clock inputs": fixed at 8 ns on 72 channels
- State analysis "1 to 8 clock inputs": fixed at 4 ns on 36 channels
- State analysis "1 to 8 clock inputs": fixed at 4 ns on 16 channels
- State analysis "clock on A16/etc...": 1 input clock period

Sequence levels

- 16 levels
- 6 If/Else lines per level
- 1 default "else" line per level
- 4 value events per level
- 2 edges events per level
- 2 ranges events per level
- 2 timers/counters per level

Trigger events

- 16 value events
- 8 edge events
- 8 range events (up to 36-bit values)

Actions

- Trigger
- Goto Level

Glitch triggers

- Available in Glitch timing mode
- Channels which trigger on glitches can be selected
- Simple, Series, and Timebetween always trigger on selected glitch channels
- Custom TriggerForm allows specific sequence levels to trigger on glitches

Selective storage

- Store all data while on a level, no data, or specified patterns
- Available in Timing and State modes

Timers/counters

- Two 36-bit timers/counters per level
- See Appendix C for limits

Trigger-out signal

- Falling edge signal on trigger
- 3V when the logic analyzer starts running
- Changes from 3V to 0V when the logic analyzer triggers

Serial bus trigger and decode

- 1-wire: Command plus up to 5 bytes
- CAN/CAN-FD: Full header plus up to 5 bytes
- I2C: up to 9 bytes
- I2S: up to 8 bytes
- LIN: Full header plus up to 6 bytes
- Raw bit-stream: up to 8 bytes
- SD / SDIO / MMC / eMMC: Full header plus up to 8 bytes
- SPI / Micro-wire: up to 8 bytes
- SPI Multi-IO: Full header plus up to 6 bytes
- UART: up to 7 bytes

Notes: Depending on bus type, data values can be contiguous or separated by non-matching values. Some bus protocols infer that data values are always contiguous within a packet.

Also, fewer trigger values are available as the bit-width of each value increases. For example the SPI bus can be configured for 32-bit double words rather than 8-bit bytes. In that case, only 3 values can be in the trigger series.

Dimensions

Width: 3.9" (100 mm)

Length: 5.7" (145 mm)

Height: 1.6" (41 mm)

Weight (main unit alone): 21.5 oz. (608 grams)

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